Web Results **11** - **20** of about **2,740** for **memory cache queue dequeue enqueue** . (**0.13** seconds)

22C:116, Homework 4 Solutions, Spring 1997
... It needs to have allocated for it enough **memory** space to fit in all the disk blocks. Request **queue** as a **cache** works best when there is frequent reading or ...
www.cs.uiowa.edu/~jones/opsys/spring97/hw/04sol.html - 8k - Cached - Similar pages

[PPT] An active **queue** management scheme to contain high bandwidth flows
File Format: Microsoft Powerpoint 97 - View as HTML
... 13. Partial State Approach. Similar to how **caches** are employed in computer **memory** systems. Exploit locality. ... Move flow to top of **cache**. No. Is. ... **Queue**. 39. ...
ee.tamu.edu/~reddy/presentations/partial.ppt - Similar pages

[PPT] CS 311 Lecture 3: Strings
File Format: Microsoft Powerpoint 97 - View as HTML
... v[5]. 4. v[6]. **Queue**: Wraparound. Wrap around to beginning: v[0]. v[1]. ... And so is jumping around in **memory**. Which would ruin **cache**/VM performance. The end. Next lecture. ...
ccl.northwestern.edu/tisue/cs311/ fall-00/lectures/08.ppt - Similar pages

[PPT] Scout: A Communication-Oriented Operating System
File Format: Microsoft Powerpoint 97 - View as HTML
... 21. Multiple Protected **Queues**. Output must select **queue**. Some QoS scheduling (16 priority levels). ... Hardware support. **Memory** bus. Fast **cache** access. Tradeoffs? ...
www.cs.princeton.edu/~tspalink/tspalink_CMU01.ppt - Similar pages

1. Introduction
... An efficient algorithm requires that a priority **queue** is operated in ... the LR algorithm, and the RK algorithm on a **cache** coherent shared-**memory** system. ...
www.acm.org/jea/ARTICLES/Vol3Nbr3/node1.html - 9k - Cached - Similar pages

iPlanet Messaging Server 5.2 Administrator's Guide: Chapter 5 MTA ...
... the master program can only **dequeue** messages from ... message backlogs overflow the Job Controller's in-**memory cache**. ... Controller must scan the MTA **queue** directory. ...
docs.sun.com/source/816-6009-10/mtacncpt.htm - 48k - Cached - Similar pages

[PDF] Simple, Fast, and Practical Non-Blocking and Blocking Concurrent ...
File Format: PDF/Adobe Acrobat - View as HTML
... length of the "other work" between **queue** operations. With only one processor, **memory** references in all but ... loop iteration hit in the **cache**, and completion ...
www.research.ibm.com/people/m/michael/podc-1996.pdf - Similar pages

2/458: Parallel and Distributed Systems Jan. 15-27, 2003 Why ...
... reschedule: t : cb := **dequeue**(ready_list) transfer(t) To ... locks optimizations allocate stacks lazily **cache memory** blocks of ... SC; don't need locks **queue** of idle ...
www.cs.rochester.edu/u/scott/458/notes/01-threads - 11k - Cached - Similar pages

[PPT] Orca
File Format: Microsoft Powerpoint 97 - View as HTML
... CPU. **cache**/. **memory**. ... 7. Distributed Shared **Memory**(3). Languages and libraries. ... object implementation JobQueue;. Q: "**queue** of jobs";. operation addjob(j: job);. ...

h g gec e ch e c che e e e e e e e h e

www.cs.vu.nl/pub/bal/neworca3.ppt - Similar pages
[More results from www.cs.vu.nl]

[PDF] CKRM: Class-based Prioritized Resource Control in Linux
File Format: PDF/Adobe Acrobat - View as HTML
... CPU Control in CKRM • **Memory** • I/O ... by process priority • Operations (**enqueue**, **dequeue**, get_next_task) are O ... Switch active and expired **queue** when all tasks ...
ckrm.sourceforge.net/documentation/ ckrm-ols03-presentation.pdf - Similar pages

◀ Goooooooooogle ▶
Result Page: **Previous** 1 2 3 4 5 6 7 8 9 1011 **Next**

memory cache queue dequeue enqu Search

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h g gec e ch e c che e e e e e e e e h e

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, April 29, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L79	(memory and queue$ and dequeu$).ti.	6
		DB=USPT; PLUR=YES; OP=ADJ	
☐	L78	US-6668307-B1.did.	1
☐	L77	US-6668307-B1.did.	1
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L76	L75 and (fetch$ near5 pointer$1)	1
☐	L75	(memory and cache and structure).ti.	102
☐	L74	L73 and (fetch$ near5 cache)	1
☐	L73	L72 and (empty near5 queue)	8
☐	L72	L71 and updat$	16
☐	L71	L70 and commands	17
☐	L70	L69 and enqueu$	17
☐	L69	L68 and dequeue$	18
☐	L68	L67 and (fetch$ near5 memory)	48
☐	L67	L66 and ((head near5 tail) same (pointer$1))	170
☐	L66	queue near5 descriptors	908
☐	L65	L64 and descriptor$1	2
☐	L64	(cache and memory and queu$).ti.	58
☐	L63	L62 and header	9
☐	L62	L61 and enqueue$	25
☐	L61	L60 and (memory near5 dequeue$)	30
☐	L60	'memory queue'	1150
☐	L59	6438651 .uref.	2
☐	L58	(queu$ and dequeu$ and cache).ti.	3
☐	L57	l11 and l2	2
☐	L56	L55 and (enqueu$ near5 operation$1)	11
☐	L55	L54 and (dequeue near5 operation$1)	11
☐	L54	L53 and (fetch$ near5 memory)	11
☐	L53	L52 and (head same tail)	14
☐	L52	L51 and pointer$1	15
☐	L51	L50 and cache	15

h e b b cg b chh e gf e f c e ch

☐	L50	L49 and command$1	15
☐	L49	L48 and (queue near5 descriptor$1)	18
☐	L48	L47 and (enqueue$ near5 memory)	83
☐	L47	L46 and (deque$ near5 memory)	165
☐	L46	memory near5 queue$	9947
☐	L45	L44 and ((dequeu$ or enque$) same (commands))	1
☐	L44	(memory and queue and device$1).ti.	75
☐	L43	L42 and ((modif$ or updat$) near5 (descriptor$1))	9
☐	L42	L41 and cache	21
☐	L41	L40 and (queue near5 descriptor$1)	21
☐	L40	L38 and ((command$1) same (dequeue or enqueue))	38
☐	L39	L38 and (command$1 near5 enqueue)	15
☐	L38	L37 and (tail near5 pointer$1)	549
☐	L37	L36 and (head near5 pointer$1)	744
☐	L36	memory near5 queue	9372
☐	L35	(memory and queue and array$).ti.	7
☐	L34	L33 and empty	4
☐	L33	L32 and enqueue	7
☐	L32	L31 and (tail near5 pointer$1)	7
☐	L31	L30 and (modify$ or updat$)	7
☐	L30	L29 and bit$1	7
☐	L29	L28 and lru	9
☐	L28	L27 and pointer$1	10
☐	L27	L26 and head	10
☐	L26	L25 and commands	10
☐	L25	L24 and pointer$1	10
☐	L24	L23 and dequeue	11
☐	L23	L22 and enqueue	22
☐	L22	(queue near5 descriptor$1) same (memory near5 cache)	40
☐	L21	5471604 .uref.	5
☐	L20	L18 and (counter$1 same pointer$1)	1
☐	L19	L18 and (counter$1 same queue)	0
☐	L18	(memory and header and pointer$1).ti.	15
☐	L17	5268900 .uref.	83
☐	L16	L15 and bit$1	0
☐	L15	L14 and dequeu$	2
☐	L14	(network$ and device$1 and memory and queu$).ti.	12

h e b b cg b chh e gf e f c e ch

☐	L13	L11 and (queue$1 near5 descriptor$1)	1
☐	L12	L11 and ((queue$1) same (queues descriptor$1))	0
☐	L11	(memory and data and structure).ti.	996
☐	L10	L8 and (bit$1 same pointer$1)	3
☐	L9	L8 and pointer$1	12
☐	L8	(memory and cache and queue$).ti.	55
☐	L7	L6 and dequeue	2
☐	L6	L5 and enqueue	12
☐	L5	L4 and header	16
☐	L4	L3 and (tail near5 pointer$1)	29
☐	L3	L2 and (cache near5 pointer$)	150
☐	L2	L1 and (fetch$ near5 memory)	1572
☐	L1	(memory near5 queue)	9372

END OF SEARCH HISTORY

h e b b cg b chh e gf e f c e ch

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, April 29, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L35	(memory and queue and array$).ti.	7
☐	L34	L33 and empty	4
☐	L33	L32 and enqueue	7
☐	L32	L31 and (tail near5 pointer$1)	7
☐	L31	L30 and (modify$ or updat$)	7
☐	L30	L29 and bit$1	7
☐	L29	L28 and lru	9
☐	L28	L27 and pointer$1	10
☐	L27	L26 and head	10
☐	L26	L25 and commands	10
☐	L25	L24 and pointer$1	10
☐	L24	L23 and dequeue	11
☐	L23	L22 and enqueue	22
☐	L22	(queue near5 descriptor$1) same (memory near5 cache)	40
☐	L21	5471604 .uref.	5
☐	L20	L18 and (counter$1 same pointer$1)	1
☐	L19	L18 and (counter$1 same queue)	0
☐	L18	(memory and header and pointer$1).ti.	15
☐	L17	5268900 .uref.	83
☐	L16	L15 and bit$1	0
☐	L15	L14 and dequeu$	2
☐	L14	(network$ and device$1 and memory and queu$).ti.	12
☐	L13	L11 and (queue$1 near5 descriptor$1)	1
☐	L12	L11 and ((queue$1) same (queues descriptor$1))	0
☐	L11	(memory and data and structure).ti.	996
☐	L10	L8 and (bit$1 same pointer$1)	3
☐	L9	L8 and pointer$1	12
☐	L8	(memory and cache and queue$).ti.	55
☐	L7	L6 and dequeue	2
☐	L6	L5 and enqueue	12
☐	L5	L4 and header	16

h e b b cg b chh e gf e f c e ch

☐	L4	L3 and (tail near5 pointer$1)	29
☐	L3	L2 and (cache near5 pointer$)	150
☐	L2	L1 and (fetch$ near5 memory)	1572
☐	L1	(memory near5 queue)	9372

END OF SEARCH HISTORY

h e b b cg b chh e gf e f c e ch

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Wednesday, April 28, 2004

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
☐	L12	L11 and deque$	3
☐	L11	l3 and (queu$1 near5 descriptor$1)	14
☐	L10	(cache$ and que$ and deque$).ti.	0
☐	L9	(memory and que$ and deque$).ti.	0
☐	L8	(memory and cache$ and que$ and deque$).ti.	0
☐	L7	L6 and bit$1	2
☐	L6	L5 and deque$	3
☐	L5	L4 and pointer$1	18
☐	L4	L3 and (cach$ near5 operation$1)	32
☐	L3	(memory$ and queu$).ti.	730
☐	L2	L1 and (cache near5 operation$1)	1
☐	L1	(queu$ and memory and head$).ti.	15

END OF SEARCH HISTORY

h e b b cg b chh e f c e ch

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20030046414 A1

Using default format because multiple data bases are involved.

L12: Entry 1 of 3 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046414
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046414 A1

TITLE: Operation of a multiplicity of time sorted queues with reduced memory

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Pettyjohn, Ronald L.	Concord	MA	US	
Milliken, Walter C.	Dover	NH	US	

US-CL-CURRENT: 709/230; 709/250

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20030131198 A1

L12: Entry 2 of 3 File: DWPI Jul 10, 2003

DERWENT-ACC-NO: 2003-709485
DERWENT-WEEK: 200367
COPYRIGHT 2004 DERWENT INFORMATION LTD
TITLE: Queue array caching method executed in processor for network devices, e.g. routers, involves referencing queue descriptor stored in cache in processor's memory controller logic to execute enqueue and dequeue operations

INVENTOR: BERNSTEIN, D; ROSENBLUTH, M B ; WOLRICH, G

PRIORITY-DATA: 2002US-0041678 (January 7, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20030131198 A1	July 10, 2003		008	G06F012/00

INT-CL (IPC): G06 F 12/00

h e b b g e e e f e ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 3. Document ID: US 20030131022 A1

L12: Entry 3 of 3 File: DWPI Jul 10, 2003

DERWENT-ACC-NO: 2003-662239
DERWENT-WEEK: 200362

TITLE: Enqueuing and dequeuing method, involves fetching head or tail pointer from memory to cache based on enqueue or dequeue operation in response to command and returning memory from cache portions of queue descriptor

INVENTOR: BERNSTEIN, D; ROSENBLUTH, M B ; WOLRICH, G

PRIORITY-DATA: 2002US-0039289 (January 4, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20030131022 A1	July 10, 2003		012	G06F007/00

INT-CL (IPC): G06 F 7/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
DEQUE$	0
DEQUE	81
DEQUEAT	1
DEQUEBEE	1
DEQUECH	1
DEQUECKER	2
DEQUECKER-P	1
DEQUECKER-PHILIPPE	1
DEQUED	15
DEQUEDE	5
(L11 AND DEQUE$).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	3

There are more results than shown above. Click here to view the entire set.

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 5809550 A

Using default format because multiple data bases are involved.

L10: Entry 1 of 3 File: USPT Sep 15, 1998

US-PAT-NO: 5809550
DOCUMENT-IDENTIFIER: US 5809550 A

TITLE: Method and apparatus for pushing a cacheable memory access operation onto a bus controller queue while determining if the cacheable memory access operation hits a cache

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shukla; Rahul	Tempe	AZ		
Heeb; Jay	Gilbert	AZ		
Jehl; Timothy	Chandler	AZ		

US-CL-CURRENT: 711/167; 711/118, 711/135, 711/138, 711/168

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw De

☐ 2. Document ID: US 5748932 A

L10: Entry 2 of 3 File: USPT May 5, 1998

US-PAT-NO: 5748932
DOCUMENT-IDENTIFIER: US 5748932 A

TITLE: Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence

DATE-ISSUED: May 5, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Van Dyke; Korbin S.	Fremont	CA		
Stiles; David R.	Sunnyvale	CA		

h e b b g e e e f e gf e ef b e

Favor; John G. San Jose CA

US-CL-CURRENT: 715/526; 711/100

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 5230068 A

L10: Entry 3 of 3 File: USPT Jul 20, 1993

US-PAT-NO: 5230068
DOCUMENT-IDENTIFIER: US 5230068 A

TITLE: Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence

DATE-ISSUED: July 20, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Van Dyke; Korbin S.	Fremont	CA		
Stiles; David R.	Sunnyvale	CA		
Favor; John G.	San Jose	CA		

US-CL-CURRENT: 711/137

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
BIT$1	0
BIT	622119
BITA	217
BITB	205
BITC	158
BITD	158
BITE	49434
BITF	78
BITG	207
BITH	1624
BITI	2040
(L8 AND (BIT$1 SAME	3

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5101494 A

Using default format because multiple data bases are involved.

L13: Entry 1 of 1 File: USPT Mar 31, 1992

US-PAT-NO: 5101494
DOCUMENT-IDENTIFIER: US 5101494 A

TITLE: System for producing memory maps by interpreting a descriptor file which identifies and describes the data structures present in memory

DATE-ISSUED: March 31, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bilski; Maryann J.	Waltham	MA		
Vermilion; Edson O.	Windham	NH		
Chang; Jang-Li	Dracut	MA		

US-CL-CURRENT: 717/127; 711/1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
QUEUE$1	0
QUEUE	52625
QUEUEA	2
QUEUEC	1
QUEUED	15956
QUEUEE	3
QUEUEG	1
QUEUEH	1
QUEUEI	2
QUEUEJ	1

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 20030131198 A1

Using default format because multiple data bases are involved.

L15: Entry 1 of 2 File: DWPI Jul 10, 2003

DERWENT-ACC-NO: 2003-709485
DERWENT-WEEK: 200367
COPYRIGHT 2004 DERWENT INFORMATION LTD
TITLE: Queue array caching method executed in processor for network devices, e.g. routers, involves referencing queue descriptor stored in cache in processor's memory controller logic to execute enqueue and dequeue operations

INVENTOR: BERNSTEIN, D; ROSENBLUTH, M B ; WOLRICH, G

PRIORITY-DATA: 2002US-0041678 (January 7, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20030131198 A1	July 10, 2003		008	G06F012/00

INT-CL (IPC): G06 F 12/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: WO 9301670 A1, EP 593534 A4, AU 9221858 A, US 5268900 A, EP 593534 A1, AU 652469 B

L15: Entry 2 of 2 File: DWPI Jan 21, 1993

DERWENT-ACC-NO: 1993-045792
DERWENT-WEEK: 199842
COPYRIGHT 2004 DERWENT INFORMATION LTD
TITLE: High-speed queuing discipline implementing device for prioritisation in packet network - is based on scan table-based dequeueing scheme using pre-computed scan table stored in memory

INVENTOR: BHARGAVA, A; HLUCHYJ, M G

PRIORITY-DATA: 1991US-0726065 (July 5, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC

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Hit List

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5471604 A

Using default format because multiple data bases are involved.

L20: Entry 1 of 1 File: USPT Nov 28, 1995

US-PAT-NO: 5471604
DOCUMENT-IDENTIFIER: US 5471604 A
**** See image for Certificate of Correction ****

TITLE: Method for locating sector data in a memory disk by examining a plurality of headers near an initial pointer

DATE-ISSUED: November 28, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hasbun; Robert N.	Shingle Springs	CA		
Wells; Stephen	Citrus Heights	CA		

US-CL-CURRENT: 711/4; 711/1, 711/105, 711/112

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
COUNTER$1	0
COUNTER	933663
COUNTERA	434
COUNTERB	1091
COUNTERC	1054
COUNTERD	43
COUNTERE	624
COUNTERF	119
COUNTERG	66
COUNTERH	7

h e b b g e e e f e gf e ef b e

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 20040034743 A1

Using default format because multiple data bases are involved.

L34: Entry 1 of 4 File: PGPB Feb 19, 2004

PGPUB-DOCUMENT-NUMBER: 20040034743
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040034743 A1

TITLE: Free list and ring data structure management

PUBLICATION-DATE: February 19, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	
Bernstein, Debra	Sudbury	MA	US	
Sweeney, John	Harvard	MA	US	
Guilford, James D.	Northborough	MA	US	

US-CL-CURRENT: 711/132; 711/133

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030140196 A1

L34: Entry 2 of 4 File: PGPB Jul 24, 2003

PGPUB-DOCUMENT-NUMBER: 20030140196
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030140196 A1

TITLE: Enqueue operations for multi-buffer packets

PUBLICATION-DATE: July 24, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	

h e b b g e e e f e gf e ef b e

Bernstein, Debra	Sudbury	MA	US

US-CL-CURRENT: 711/118; 711/154

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20030131022 A1

L34: Entry 3 of 4 File: PGPB Jul 10, 2003

PGPUB-DOCUMENT-NUMBER: 20030131022
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030131022 A1

TITLE: Queue arrays in network devices

PUBLICATION-DATE: July 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	
Bernstein, Debra	Sudbury	MA	US	

US-CL-CURRENT: 707/200

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20030115347 A1

L34: Entry 4 of 4 File: PGPB Jun 19, 2003

PGPUB-DOCUMENT-NUMBER: 20030115347
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030115347 A1

TITLE: Control mechanisms for enqueue and dequeue operations in a pipelined network processor

PUBLICATION-DATE: June 19, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	
Bernstein, Debra	Sudbury	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 709/230; 711/101, 711/169

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Hit List

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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 20040008714 A1

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L35: Entry 1 of 7 File: DWPI Jan 15, 2004

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DERWENT-WEEK: 200412
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TITLE: Packet buffer RAM for computer network, stores packet data received from multiple input/output ports in memory using serial registers divided into segments that are associated with respective queue of memory array

INVENTOR: JONES, D E

PRIORITY-DATA: 1998US-080362P (April 1, 1998), 1999US-0283778 (March 31, 1999), 2003US-0614558 (July 7, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040008714 A1	January 15, 2004		028	H04L012/54

INT-CL (IPC): H04 L 12/54

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 20030131198 A1

L35: Entry 2 of 7 File: DWPI Jul 10, 2003

DERWENT-ACC-NO: 2003-709485
DERWENT-WEEK: 200367
COPYRIGHT 2004 DERWENT INFORMATION LTD
TITLE: Queue array caching method executed in processor for network devices, e.g. routers, involves referencing queue descriptor stored in cache in processor's memory controller logic to execute enqueue and dequeue operations

INVENTOR: BERNSTEIN, D; ROSENBLUTH, M B ; WOLRICH, G

PRIORITY-DATA: 2002US-0041678 (January 7, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC

h e b b g e e e f e gf e ef b e

US 20030131198 A1 July 10, 2003 008 G06F012/00

INT-CL (IPC): G06 F 12/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

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3. Document ID: TW 522558 A, JP 2002184874 A, KR 2002046139 A

L35: Entry 3 of 7 File: DWPI Mar 1, 2003

DERWENT-ACC-NO: 2002-562562
DERWENT-WEEK: 200365
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TITLE: Semiconductor device e.g. flash memory for portable apparatus, consists of memory cell array that arranges semiconductor memory elements having charge storage areas adjacent to channel area in shape of queue

PRIORITY-DATA: 2000JP-0375686 (December 11, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 522558 A	March 1, 2003		000	H01L027/115
JP 2002184874 A	June 28, 2002		030	H01L021/8247
KR 2002046139 A	June 20, 2002		000	H01L027/115

INT-CL (IPC): H01 L 21/8247; H01 L 27/115; H01 L 29/788; H01 L 29/792

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

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4. Document ID: EP 897154 A2, US 6134638 A, JP 11167514 A

L35: Entry 4 of 7 File: DWPI Feb 17, 1999

DERWENT-ACC-NO: 1999-134338
DERWENT-WEEK: 200054
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TITLE: Computer system with memory having SDRAM array - has multiple memory clock frequencies provided by memory controller and uses asynchronous data queues to transfer data to processor and peripheral buses

INVENTOR: OLARIG, S P; PETTEY, C J

PRIORITY-DATA: 1997US-0910847 (August 13, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 897154 A2	February 17, 1999	E	019	G06F013/16
US 6134638 A	October 17, 2000		000	G06F013/16
JP 11167514 A	June 22, 1999		017	G06F012/00

INT-CL (IPC): G06 F 1/06; G06 F 12/00; G06 F 13/16; G06 F 13/368

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 5. Document ID: WO 9735400 A2, KR 99014881 A, EP 827656 A2, WO 9735400 A3, US 5917482 A, JP 11507188 W

L35: Entry 5 of 7 File: DWPI Sep 25, 1997

DERWENT-ACC-NO: 1997-480508
DERWENT-WEEK: 200018
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TITLE: Data synchronisation system for sequencing field based data - has data queues and memory array which outputs and inputs multiple data streams which are held in synchronisation using ideal queues for field sequences

INVENTOR: PUTNAM, L; PUTNAM, L K

PRIORITY-DATA: 1996US-0616950 (March 18, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 9735400 A2	September 25, 1997	E	031	H04L007/02
KR 99014881 A	February 25, 1999		000	H04L007/00
EP 827656 A2	March 11, 1998	E	000	H04L007/02
WO 9735400 A3	October 23, 1997		000	H04L007/02
US 5917482 A	June 29, 1999		000	H04N005/04
JP 11507188 W	June 22, 1999		037	H04N005/93

INT-CL (IPC): G11 B 20/10; H04 L 7/00; H04 L 7/02; H04 N 5/04; H04 N 5/765; H04 N 5/781; H04 N 5/93

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: CN 1122043 A

L35: Entry 6 of 7 File: DWPI May 8, 1996

DERWENT-ACC-NO: 1997-490524
DERWENT-WEEK: 199746
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TITLE: Memory array queue device - has counter to count data digits in shift register and to control output position selection of multiplexer

INVENTOR: DENG, Y

PRIORITY-DATA: 1994CN-0115285 (September 16, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
CN 1122043 A	May 8, 1996		001	G11C008/04

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INT-CL (IPC): G11 C 8/04

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

7. Document ID: US 5058051 A

L35: Entry 7 of 7 File: DWPI Oct 15, 1991

DERWENT-ACC-NO: 1991-324794
DERWENT-WEEK: 199144

TITLE: Address register processor system for multiple-port memory - has controller connected to data queue into memory array for timing read-write cycles, and data output receiver

INVENTOR: BROOKS, T K

PRIORITY-DATA: 1988US-0225742 (July 29, 1988)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5058051 A	October 15, 1991		000	

INT-CL (IPC): G06F 13/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
MEMORY	1457610
MEMORIES	172235
MEMORYS	184
QUEUE	52625
QUEUES	21738
ARRAY$	0
ARRAY	642528
ARRAYA	16
ARRAYABILITY	2
ARRAYABLE	74
((MEMORY AND QUEUE AND ARRAY$).TI.).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	7

There are more results than shown above. Click here to view the entire set.

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 11 of 11 returned.

☐ 1. Document ID: US 20030131198 A1

Using default format because multiple data bases are involved.

L56: Entry 1 of 11 File: PGPB Jul 10, 2003

PGPUB-DOCUMENT-NUMBER: 20030131198
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030131198 A1

TITLE: Queue array caching in network devices

PUBLICATION-DATE: July 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	
Bernstein, Debra	Sudbury	MA	US	

US-CL-CURRENT: 711/136; 711/108

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030131022 A1

L56: Entry 2 of 11 File: PGPB Jul 10, 2003

PGPUB-DOCUMENT-NUMBER: 20030131022
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030131022 A1

TITLE: Queue arrays in network devices

PUBLICATION-DATE: July 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wolrich, Gilbert	Framingham	MA	US	
Rosenbluth, Mark B.	Uxbridge	MA	US	
Bernstein, Debra	Sudbury	MA	US	

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US-CL-CURRENT: 707/200

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 3. Document ID: US 20030061332 A1

L56: Entry 3 of 11 File: PGPB Mar 27, 2003

PGPUB-DOCUMENT-NUMBER: 20030061332
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030061332 A1

TITLE: Multiple consumer-multiple producer rings

PUBLICATION-DATE: March 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Narad, Charles E.	Santa Clara	CA	US	
Fall, Kevin	Berkeley	CA	US	
MacAvoy, Neil	Redwood City	CA	US	
Shankar, Pradip	Fremont	CA	US	
Rand, Leonard M.	San Francisco	CA	US	
Hall, Jerry J.	Santa Clara	CA	US	

US-CL-CURRENT: 709/223

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 4. Document ID: US 20030046423 A1

L56: Entry 4 of 11 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046423
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046423 A1

TITLE: Programmable system for processing a partitioned network infrastructure

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Narad, Charles E.	Santa Clara	CA	US	
Fall, Kevin	Berkeley	CA	US	
MacAvoy, Neil	Redwood City	CA	US	
Shankar, Pradip	Fremont	CA	US	
Rand, Leonard M.	San Francisco	CA	US	
Hall, Jerry J.	Santa Clara	CA	US	

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US-CL-CURRENT: 709/238

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 5. Document ID: US 20030005103 A1

L56: Entry 5 of 11 File: PGPB Jan 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030005103
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030005103 A1

TITLE: Cumulative status of arithmetic operations

PUBLICATION-DATE: January 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Narad, Charles E.	Santa Clara	CA	US	
Fall, Kevin	Berkeley	CA	US	
MacAvoy, Neil	Redwood City	CA	US	
Shankar, Pradip	Fremont	CA	US	
Rand, Leonard M.	San Francisco	CA	US	
Hall, Jerry J.	Santa Clara	CA	US	

US-CL-CURRENT: 709/223; 709/201

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 6. Document ID: US 6701338 B2

L56: Entry 6 of 11 File: USPT Mar 2, 2004

US-PAT-NO: 6701338
DOCUMENT-IDENTIFIER: US 6701338 B2

TITLE: Cumulative status of arithmetic operations

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

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US-CL-CURRENT: 708/525; 709/223

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 7. Document ID: US 6625689 B2

L56: Entry 7 of 11 File: USPT Sep 23, 2003

US-PAT-NO: 6625689
DOCUMENT-IDENTIFIER: US 6625689 B2

TITLE: Multiple consumer-multiple producer rings

DATE-ISSUED: September 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 711/110

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 8. Document ID: US 6421730 B1

L56: Entry 8 of 11 File: USPT Jul 16, 2002

US-PAT-NO: 6421730
DOCUMENT-IDENTIFIER: US 6421730 B1

TITLE: Programmable system for processing a partitioned network infrastructure

DATE-ISSUED: July 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 709/236

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 9. Document ID: US 6401117 B1

L56: Entry 9 of 11 File: USPT Jun 4, 2002

US-PAT-NO: 6401117
DOCUMENT-IDENTIFIER: US 6401117 B1
** See image for Certificate of Correction **

TITLE: Platform permitting execution of multiple network infrastructure applications

DATE-ISSUED: June 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 709/223

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 10. Document ID: US 6157955 A

L56: Entry 10 of 11 File: USPT Dec 5, 2000

US-PAT-NO: 6157955
DOCUMENT-IDENTIFIER: US 6157955 A

TITLE: Packet processing system including a policy engine having a classification unit

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

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US-CL-CURRENT: 709/228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

11. Document ID: US 20030131022 A1

L56: Entry 11 of 11 File: DWPI Jul 10, 2003

DERWENT-ACC-NO: 2003-662239
DERWENT-WEEK: 200362

TITLE: Enqueuing and dequeuing method, involves fetching head or tail pointer from memory to cache based on enqueue or dequeue operation in response to command and returning memory from cache portions of queue descriptor

INVENTOR: BERNSTEIN, D; ROSENBLUTH, M B ; WOLRICH, G

PRIORITY-DATA: 2002US-0039289 (January 4, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20030131022 A1	July 10, 2003		012	G06F007/00

INT-CL (IPC): G06 F 7/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
ENQUEU$	0
ENQUEU	4
ENQUEUCING	2
ENQUEUE	1380
ENQUEUEABLE	1
ENQUEUECOMMIT	1
ENQUEUED	2020
ENQUEUEDATA	1
ENQUEUED-AN	1
ENQUEUED-TO	5
(L55 AND (ENQUEU$ NEAR5 OPERATION$1)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	11

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